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REMARKS

A Request for Drawings Change is being filed concurrently herewith. Claims 1, 4-7, 9-22, 24-27 and 29-31 are currently pending in the above-identified application. Claims 32-39 have been withdrawn from consideration. Claims 1-31 have been rejected. Claims 1, 15, 22, 27 and 29 have been amended, while claims 2, 3, 23 and 28 have been canceled solely for the purpose of furthering the prosecution of the present application. Applicant respectfully reserves the right to claim the subject matter of the canceled and pre-amendment claims in this or any other application. Applicant respectfully requests reconsideration in light of the foregoing amendments and following remarks.

The drawings have been objected to as failing to comply with 37 C.F.R. 1.84. Specifically, reference character 22 has been used to designate first and second adhesive layers, reference character 24 has been used to designate a cavity and adhesive fillets, reference character 40 has been used to designate wire bonds and a third semiconductor die, and reference number 46 is not discussed in the specification.

A Request for Drawings Change is included with this submission. The figures to be changed include FIGS. 1-3, 5 and 7. Specifically, reference character has been changed in the drawings and the specification to 22_a and 22_b to designate, respectively, the first adhesive layer and the second adhesive layer. Reference character 24 has been changed to 24_a and 24_b to designate, respectively, an adhesive fillet between the support structure and the first semiconductor die and an adhesive fillet between the first semiconductor die and a second semiconductor die. The cavity has been denoted by the reference character 25. The third semiconductor die has been denoted by the reference character 45, and the

reference character 46 has been removed from FIG. 7. The drawings should now be in full compliance with 37 C.F.R. 1.84.

The specification has been objected to for various informalities found on page 6, line 11, page 7, line 21 and page 8, line 16. Applicant has made corrections as suggested by the Office action.

Claims 1, 15 and 27 stand rejected under 35 U.S.C. §102(b) as being anticipated by Tsubonoya and under 35 U.S.C. §102(e) as being anticipated by Chin. Applicant respectfully traverses these rejections.

The claims of the present application are directed to a semiconductor assembly which utilizes a film as a support structure for a semiconductor die and which includes adhesive material between the support structure and the semiconductor die that does not extend beyond the perimeter of the semiconductor die. This arrangement allows for a semiconductor assembly that is both thinner and has a smaller footprint, since the absence of adhesive outside the perimeter of the semiconductor die allows for a good border for making a wire bond without having to increase the area of the support structure. In some claims, the distance between an electrical contact area on the support structure and the perimeter of the semiconductor die is defined to be less than or equal to 428 microns, and may indeed be less than or equal to 200 microns.

Claim 1, as amended, recites a semiconductor assembly that includes "a support structure having a top surface, wherein said support structure is a film" and "at least one semiconductor die having a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure, said at least one semiconductor die

being secured at its bottom surface to said top surface of said support structure by a flowable adhesive material which does not extend past a perimeter of said at least one semiconductor die".

Claim 15, as amended recites a semiconductor assembly that includes "a first semiconductor die having a top and a bottom surface", "a second semiconductor die having a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die, said second die being secured at its bottom surface to said top surface of said first semiconductor die by a flowable adhesive material which does not extend past a perimeter of said second semiconductor die" and "wherein said top surface of said first semiconductor die has at least one electrical contact area positioned at a location exterior to said perimeter of said second semiconductor die, and wherein a distance between said electrical contact area and said perimeter of said second semiconductor die is less than or equal to about 428 microns".

Claim 27, as amended, recites semiconductor assembly that includes "a support structure", "a first semiconductor die having a top and bottom surface, said bottom surface being secured to said support structure", "a second semiconductor die having a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die, said second die being secured at its bottom surface to said top surface of said first semiconductor die by a flowable adhesive material which does not extend past a perimeter of said second die" and "wherein said top surface of said first semiconductor die has at least one electrical contact area positioned at a location exterior to said perimeter of said second semiconductor die, and wherein a distance between said electrical contact area

and said perimeter of said second semiconductor die is less than or equal to about 428 microns".

Tsubonoya discloses a support structure 3, semiconductor dies 1a and 1b, and an adhesive material between the support structure and the semiconductor dies. Tsubonoya fails to teach or suggest "a support structure having a top surface, wherein said support structure is a film" as recited in claim 1, and "said first semiconductor die has at least one electrical contact area positioned at a location exterior to said perimeter of said second semiconductor die, and wherein a distance between said electrical contact area and said perimeter of said second semiconductor die is less than or equal to about 428 microns" as recited in claims 15 and 27. The use of a film as a substrate provides a thinner semiconductor assembly. The claimed use of an adhesive which does not extend past a perimeter of a die and the claimed distance between the perimeter of the die and an electrical contact area on the support structure of less than 428 microns provide a semiconductor assembly with a smaller footprint. Since Tsubonoya fails to teach or suggest each and every element of claims 1, 15 and 27, these claims cannot be anticipated by this reference.

Chin discloses a support structure 8, first and second semiconductor dies 7a and 7b, and an adhesive material. Chin, like Tsubonoya, fails to teach or suggest "a support structure having a top surface, wherein said support structure is a film" as recited in claim 1, and "said first semiconductor die has at least one electrical contact area positioned at a location exterior to said perimeter of said second semiconductor die, and wherein a distance between said electrical contact area and said perimeter of said second

semiconductor die is less than or equal to about 428 microns" as recited in claims 15 and 27. Since Chin fails to teach or suggest each and every element of claims 1, 15 and 27, these claims cannot be anticipated by this reference.

Claims 1-7, 10-19, 21, 27, 30 and 31 stand rejected under 35 U.S.C. §102(e) as being anticipated by Fukui et al. Applicant respectfully traverses the rejection.

Fukui et al. discloses a circuit board 5, first and second semiconductor dies 1 and 2, and an adhesive material 6 between the support structure and the semiconductor dies. Fukui et al., like Tsubonoya and Chin, fails to teach or suggest "a support structure having a top surface, wherein said support structure is a film" as recited in independent claim 1, and "said first semiconductor die has at least one electrical contact area positioned at a location exterior to said perimeter of said second semiconductor die, and wherein a distance between said electrical contact area and said perimeter of said second semiconductor die is less than or equal to about 428 microns" as recited in independent claims 15 and 27. Since Fukui et al. fails to teach or suggest each and every element of claims 1, 15 and 27, as well as dependent claims 4-7, 10-14, 16-19, 21, 30 and 31, this reference does not anticipate these claims.

Claims 22-24 and 26 stand rejected under 25 U.S.C. §102(e) as being anticipated by Hawke et al. Applicant respectfully traverses the rejection.

Claims 22, 24 and 26, as amended, recite a semiconductor assembly that includes "a first semiconductor die having a top and a bottom surface", "a support structure to which said bottom surface of said first semiconductor die is secured, wherein said support structure is a film", " a second semiconductor die having a top and a bottom

surface, said bottom surface having a smaller area than said top surface of said first semiconductor die" and "a third semiconductor die having a top and a bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die, said second and third semiconductor dies being secured at their bottom surface to said top surface of said first semiconductor die by a flowable adhesive material which does not extend past a perimeter of said second semiconductor die or said third semiconductor die".

Hawke et al. discloses a semiconductor assembly which includes a first IC layer 208 resident upon a substrate 202, a second IC layer 216 on the first IC layer 208, and a third IC layer 218 made up of ICs 218a and 218b. However, Hawke et al. fails to teach or suggest "a support structure to which said bottom surface of said first semiconductor die is secured, wherein said support structure is a film" as recited in claims 22-24 and 26. As noted earlier, the use of a film as a substrate provides a thinner semiconductor assembly. The use of an adhesive which does not extend past a perimeter of a die and having a distance between the perimeter of the semiconductor die(s) and an electrical contact area on the support structure of less than 428 microns provides a semiconductor assembly with a smaller footprint. Since Hawke et al. fails to teach or suggest each and every element of claims 22, 24 and 26, these claims cannot be anticipated by this reference.

Claims 8, 9, 20, 28 and 29 stand rejected under 35 U.S.C. §103 as being unpatentable over Fukui et al. in view of Ball. Claim 28 has been canceled rendering this rejection moot as to that claim. Applicant respectfully traverses the rejection.

The deficiencies of Fukui et al. with respect to the limitations of independent claims 1, 15 and 27 have been noted earlier. Ball is relied upon in the Office action for

allegedly showing a distance between the electrical contact area on the top surface of the support structure and the perimeter of the second semiconductor die is less than or equal to 200 microns, citing specifically Figure 2 of Ball. Ball illustrates in Figure 2 wires 30 bonded to lead fingers 28 and to various dies 12, 14, 16, 18 and 20. Each of the dies has the same perimeter as the other dies and each of the wires 30 is bonded to the dies at bonding sites interior to the perimeters of the dies.

Ball and Fukui et al. fail to teach or suggest "a distance between an electrical contact area and said perimeter of said at least one semiconductor die is less than or equal to about 428 microns" as recited in claim 8, "a distance between an electrical contact area and said perimeter of said at least one semiconductor die is less than or equal to about 200 microns" as recited in claim 9, "wherein said top surface of said first semiconductor die has at least one electrical contact area positioned at a location exterior to said perimeter of said second semiconductor die" as recited in claims 20 and 29, and "wherein a distance between said electrical contact area and said perimeter of said second semiconductor die is less than or equal to about 428 microns" as recited in claims 20 and 29. Fukui et al fails to disclose any distances, while Ball only discloses various thicknesses, such as, for example, the die thickness 54 (0.012 inches or 308 microns).

Claim 25 stands rejected under 35 U.S.C. §103 as being unpatentable over Hawke et al. in view of Ball. Applicant respectfully traverses the rejection.

The arguments provided above in reference to the rejection of claims 22, 24 and 26 are equally applicable to this rejection. Specifically, neither Hawke et al. or Ball teach or

suggest "a support structure to which said bottom surface of said first semiconductor die is secured, wherein said support structure is a film" as recited in claim 25.

For at least the reasons provided above, applicant believes that each of the presently pending claims is in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

The paragraphs beginning at page 1, lines 6 and 18, page 5, line 15, page 6, line 10, page 7, lines 4 and 14, page 8, line 16, and page 9, lines 4 and 12 have been replaced; the claim 28 has been canceled without prejudice or disclaimer to the subject matter recited therein, and, the claims 1, 15, 22, 27 and 29 have been rewritten.

Paragraphs beginning on Page 1, lines 6 and 18:

In order to reduce the size of semiconductor devices numerous techniques have been developed to vertically stack one semiconductor die, hereinafter "die", on top of another die. Figure 1 illustrates a conventional method of vertically stacking two die 20, 30 on a support structure 10, such as a printed circuit board (PCB) or other thin support structure, to form a conventional semiconductor assembly 100. The first die 20 is shown secured to a support structure 10 by an adhesive material [22] 22_a using techniques well known in the art. When the first die 20 is pressed against the support structure 10 the adhesive material [22] 22_a is partially forced outside the die's 20 perimeter 29 and forms an adhesive fillet [24] 24_a. Likewise, when the second die 30 is secured against the first die 20 by an adhesive material [22] 22_b a second adhesive fillet [24] 24_b is also formed.

Both the first die 20 and second die 30 are shown wire bonded 40 to an electrical contact area 18 on the support structure 10. The first die 20 has an electrical contact area 28, such as a bonding pad, on its top surface 26. Because adhesive fillet [24] 24_b is formed when the second die 30 is secured to the first die 20, it limits the placement of the first die's 20 electrical contact area 28. The distance B between the perimeter 39 of

the second die 30 and [the] a first die's 20 electrical contact area 28 must be increased by distance A, the width of the adhesive fillet [24] 24_b, to provide sufficient operating space for the wire bonding equipment. Typical dimensions for distances B are about 428 microns or greater to allow for adhesive fillets [24] 24_b, which are conventionally about 228 microns in width or greater. Using current wire bonding equipment, distance B between electrical contact area 28 and the perimeter of the fillet [24] 24_b can be reduced to about 200 microns or less. In other words, adhesive fillet [24] 24_b requires about 228 microns or more of first die's 20 top surface 26 on each side of the first die 20. If the adhesive fillet [24] 24_b were eliminated the space could be used either to increase the size of the second die 30 or to reduce the size of the first die 20.

Paragraph beginning on Page 5, line 15:

Referring now to the drawings, where like elements are designated by like reference numerals, Figures 2-3, illustrate a plan and elevation view respectively of a partially completed semiconductor assembly 200 in which a first semiconductor die 20 is secured to the top surface 16 of supporting structure 10, by a first adhesive layer [22] 22_a. Supporting structure 10 in an exemplary embodiment is a printed circuit board or thin film, but may be any structure suitable for supporting a semiconductor die. The supporting structure 10 is shown as having two electrical contact areas 17 on surface 16 and the first die 20 is also shown as having two electrical contact areas 28. It is to be understood that any number of electrical contact areas 17, 28 may be provided on the

support structure 10 and first die 20. Also, although Figure 2 shows the contact areas 17, 28 as recessed, they may also be formed on the surface of the support structure 10 or first die 20, respectively, and could be electrically connected to external electrical paths or to other parts of the completed semiconductor assembly 200.

Paragraph beginning on Page 6, line 10:

A second adhesive layer [22] 22_b is shown in Figure 2 as deposited on [the] a top surface 26 of the first semiconductor die 20 within an adhesive layer area defined by a perimeter 34. The second adhesive layer [22] 22_b can be deposited by techniques well-known in the art to include various patterns and coverage areas. It is to be understood that perimeter 34 is representative of an area of deposition of the second adhesive layer [22] 22_b; however it is not limiting. In accordance with the invention a sufficient amount of adhesive material [22] should be deposited to adequately secure [the] a second semiconductor die 30 (see Figures 4-5) to the first semiconductor die 20. The invention includes any coverage area or pattern that does not exceed the perimeter of the second die 30. As described below, when the second die 30 is placed and pressed on the first die 20, the adhesive layer [22] 22_b represented inside of the adhesive perimeter 34 does not extend past the profile or perimeter 39 of the second die 30 (Figures 4-5).

Paragraphs beginning on Page 7, lines 4 and 14:

Figures 4-5 show the assembly 200 after a second die 30 with electrical contact areas 38 on the die's top surface 36 is pressed against the second adhesive layer [22] 22_b located on the top surface 26 of the first die 20. A cavity [24] 25 is formed between the dies 20 and 30 and is characterized by a distance D between the perimeter 34 of the second adhesive layer [22] 22_b and the perimeter 39 of the second die 30. The distance D may be a regular or irregular distance around the periphery of the adhesive layer [22] 22_b. It is to be understood that formation of cavity [24] 25 is not essential, what is important is that adhesive layer [22] 22_b does not extend beyond the perimeter 39 of the second die 30 such that no adhesive fillet 24 is formed.

If cavity [24] 25 is present, the distance D is preferably in the range such that between about 50 and about 90 percent of the second die 30 bottom surface is covered by the second adhesive material layer [22] 22_b. Figures 4 and 5 show distance C between the perimeter 39 of the second die 30 and the perimeter 29 of the first die 20. This distance is a value which provides acceptable clearance between electrical contact area 28 and the second die 30 to enable the formation of electrical contacts between the dies 20, 30 and other parts of the assembly [20] 200 such as wire bonds 40 between the dies 20, 30 and the support structure 10 (Figure[s] 6). An exemplary distance C between the perimeters 29, 39 of the first die 20 and second die 30 is about 200 microns or less. The distance C is currently only limited by the technology of the wire bond equipment and the minimum required operating space.

Paragraph beginning on Page 8, line 16:

Also shown are [the] balls 60 which make up a ball grid array pattern for making electrical connections between the support structure 10 and external electrical circuits. The balls 60 are deposited on the support structure 10 using materials and techniques well known in the art and are electrically connected through conductors supported by support structure 10 to the contact areas 17. It is to be understood that multiple semiconductor assemblies 200 could be prepared at one time on a continuous support structure 10, which could be separated into individual or multiple semiconductor assemblies 200 at a later stage of fabrication.

Paragraphs beginning on Page 9, lines 4 and 12:

Figure 6 also shows an encapsulating material 50, such as a molding compound, deposited over the wire bonds 40, semiconductor dies 20, 30, and top surface 16 of the support structure 10. As an exemplary illustration, some of the encapsulation material 50 is shown under the second die 30 and within cavity [24] 25 (Figures 4-5) and provides support and stability to the second die 30. The encapsulating material 50 and molding techniques using it are well known in the art and not repeated herein.

Figure 7 is a cross-sectional illustration of a second exemplary embodiment of a semiconductor assembly 300 with second and third semiconductor dies 30, [40] 45 secured to a first semiconductor die 20 using the techniques described above. It is to be

understood that the elimination of the adhesive fillet [24] $\underline{24_b}$ as discussed in Figure 1 covers a wide range of semiconductor configurations involving multiple dies with various sizes, dimensions, and electrical contact techniques. The above described invention has the advantage of allowing either the size of the second and third semiconductor dies 30, [40] $\underline{45}$ to be increased or allowing the size of the first semiconductor die 20 to be reduced by eliminating the wasted space occupied by the adhesive fillet [24] $\underline{24_b}$.

Claims 2, 3, 23 and 28 are canceled.

Claims 1, 15, 22, 27 and 29 are rewritten.

1. (Amended) A semiconductor assembly comprising:

a support structure having a top surface, wherein said support structure is a film; and

at least one semiconductor die having a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure, said at least one semiconductor die being secured at its bottom surface to said top surface of said support structure by a flowable adhesive material which does not extend past [the] a perimeter of said at least one semiconductor die.

15. (Amended) A semiconductor assembly comprising:

a first semiconductor die having a top and a bottom surface; [and]

a second semiconductor die having a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die, said second die being secured at its bottom surface to said top surface of said first semiconductor die by a flowable adhesive material which does not extend past [the] a perimeter of said second semiconductor die; and

wherein said top surface of said first semiconductor die has at least one electrical contact area positioned at a location exterior to said perimeter of said second semiconductor die, and wherein a distance between said electrical contact area and said perimeter of said second semiconductor die is less than or equal to about 428 microns.

22. (Amended) A semiconductor assembly comprising:

a first semiconductor die having a top and a bottom surface;

a support structure to which said bottom surface of said first semiconductor die is secured, wherein said support structure is a film;

a second semiconductor die having a top and a bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die; and

a third semiconductor die having a top and a bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die, said second and third semiconductor dies being secured at their bottom surface to said top

surface of said first semiconductor die by a flowable adhesive material which does not extend past [the] a perimeter of said second semiconductor die or said third semiconductor die.

27. (Amended) A semiconductor assembly comprising:

a support structure;

a first semiconductor die having a top and bottom surface, said bottom surface being secured to said support structure; [and]

a second semiconductor die having a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die, said second die being secured at its bottom surface to said top surface of said first semiconductor die by a flowable adhesive material which does not extend past [the] a perimeter of said second die; and

wherein said top surface of said first semiconductor die has at least one electrical contact area positioned at a location exterior to said perimeter of said second semiconductor die, and wherein a distance between said electrical contact area and said perimeter of said second semiconductor die is less than or equal to about 428 microns.

29. (Amended) The semiconductor assembly of claim [28] 27, wherein a distance between an electrical contact area on said top surface of said first semiconductor

die and said perimeter of said second semiconductor die is less than or equal to about 200 microns.